Listing of Claims:

1. (Currently Amended) A design method of designing a multilayer semiconductor device which includes a plurality of circuit blocks formed on a semiconductor substrate, the method comprising the steps of:

registering measurement terminals as cells in design rules, together with the circuit blocks, wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device, and ~~the~~ each measurement terminal is connectable to a wiring line for connecting any two of the circuit blocks, ~~which~~ and said wiring line is formed in any layer of the semiconductor device;

planar-arranging the measurement terminals and the circuit blocks based on the design rules; and

establishing connection of each wiring line, which extends from one of the circuit blocks, via one of the measurement terminals.

2. (Currently Amended) A design method as claimed in claim 1, wherein in the step of establishing the connection of each wiring line, the connection is performed based on a net list which stores data of each measurement terminal and terminations of a wiring line on which ~~the~~ each measurement terminal is provided.

3. (Withdrawn) An inspection method of inspecting a multilayer semiconductor device which includes a plurality of circuit blocks formed on a semiconductor substrate, the method comprising the step of:

performing inspection via an electrode of a measurement terminal, wherein the measurement terminal is provided on a wiring line which extends from one of the circuit blocks, the electrode is formed in an uppermost layer of the semiconductor device, and the measurement terminal has a pad in each of the remaining layers of the semiconductor device, and the pads are electrically connected with each other via contact holes, each contact hole passing through each insulating film of the semiconductor device.

4. (Withdrawn) An inspection method as claimed in claim 3, wherein the step of performing inspection includes measuring at least one of voltage and logic state of the wiring line on a which the measurement terminal is provided, by one of making a probe contact the electrode of the measurement terminal and irradiating the electrode with an electron beam.

5. (Currently Amended) A design program for making a computer execute an operation of designing a multilayer semiconductor device which includes a plurality of circuit blocks formed on a semiconductor substrate, the operation comprising the steps of:

registering measurement terminals as cells in design rules, together with the circuit blocks, wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device, and ~~the~~ each measurement terminal is connectable to a wiring line for connecting any two of the circuit blocks, ~~which~~ and said wiring line is formed in any layer of the semiconductor device;

planar-arranging the measurement terminals and the circuit blocks based on the design rules; and

establishing connection of each wiring line, which extends from one of the circuit blocks, via one of the measurement terminals.

6. (Withdrawn) A multilayer semiconductor device which includes a plurality of circuit blocks formed on a semiconductor substrate, the semiconductor device comprises: measurement terminals, each provided on a wiring line which extends from one of the circuit blocks, wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device and a pad provided in each of the remaining layers of the semiconductor device, and the electrode and the pads are connected with each other via contact holes.

7. (Withdrawn) A multilayer semiconductor device as claimed in claim 6, wherein the positions of the electrode and the pads are substantially the same in plan view.